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March 26, 2004
AMAT/1831.P1/CPI/COPPERVPS
Examiner: Ginetta Parata
703-872-8308
USPTO
Keith M. Tackett
7

☐ YES ☒ NO

RULE 312 AMENDMENT AFTER ALLOWANCE

TITLE:
U.S. SERIAL NO.:
FILING DATE:
INVENTOR:
EXAMINER:
GROUP ART UNIT:
CONFIRMATION NO.:

Reliability Barrier Integration for CU Application
10/052,681
January 17, 2002
XJ, et al.
Ginetta Parata
2814
4083

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T-453 P.013/022 F-507

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Attorney Dkt. AMAT/1931.P1/CPI/COPPERPJS
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Xi, et al.

Serial No.: 10/052,681

Confirmation No.: 4083

Filed: January 17, 2002

For: Reliability Barrier Integration for
CU Application

Group Art Unit: 2814

Examiner: Ginette Peralta

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I hereby certify that this correspondence and the documents referred to as attached therein are being facsimile transmitted to the U.S. Patent and Trademark Office to the fax number indicated by the Examiner, namely, fax number (703) 872-9306 to the attention of the named Examiner, on the date below.

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RULE 312 AMENDMENT AFTER ALLOWANCE

Following mailing of a Notice of Allowance on December 31, 2003, Applicants request entry of the following amendment to correct the dependency of an allowed claim. Amendments to the Claims are shown in the listing of the claims beginning on page 2 of this paper. Remarks begin on page 8 of this paper.

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Atty. Dkt AMAT/1931.P1/CPI/COPPER/PJS

IN THE CLAIMS:

Please amend the claims as follows:

1. (Previously Presented) A method of filling one or more of a via and a trench in a patterned substrate, comprising:
 - a) depositing a generally conformal first barrier layer in one or more of the via and the trench on the patterned substrate by chemical vapor deposition, wherein the first barrier layer is selected from the group consisting of TiSi_xN , $\text{TiN}(\text{C})$, $\text{TiNSi}(\text{C})$, Ta, TaC, TaN(C), TaNSi(C), W, WN_x , SiO_xN_y , SiC, AlN, and Al_2O_3 ;
 - b) removing the first barrier layer from the horizontal surfaces of the patterned substrate;
 - c) depositing a second barrier layer by physical vapor deposition; and then
 - d) depositing one or more conductive materials.
2. (Original) The method of claim 1 wherein depositing the conductive material comprises depositing a seed layer and a metal layer in the via and/or the trench after the second barrier layer is deposited.
3. (Previously Presented) The method of claim 2 wherein the first barrier layer is selected from the group consisting of $\text{TiN}(\text{C})$, Ta, TaC, TaN(C), W, WN_x , SiC, AlN, and Al_2O_3 .
4. (Previously Presented) The method of claim 1 wherein the second barrier layer is selected from the group consisting of Ta, TaN, TiSiN_x , TaSiN_x , W, and WN_x .
5. (Currently Amended) The method of claim [[4]] 2 wherein the seed layer is copper.
6. (Original) The method of claim 5 wherein the metal layer is copper.

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Atty. Dkt AMAT/1931.P1/GPI/COPPER/PJS

7. (Original) The method of claim 1 wherein the first barrier layer is deposited and removed from the horizontal surfaces of the patterned substrate within a single chamber of an integrated processing tool.
8. (Original) The method of claim 7 wherein the chamber is a chemical vapor deposition chamber and the first barrier layer is deposited and etched in the chamber.
9. (Original) The method of claim 2 wherein the seed layer is deposited by physical vapor deposition.
10. (Original) The method of claim 2 wherein the seed layer is deposited by chemical vapor deposition.
11. (Original) The method of claim 2 wherein the seed layer is deposited by electroless deposition.
12. (Original) The method of claim 2 wherein the metal layer is deposited by physical vapor deposition.
13. (Original) The method of claim 2 wherein the metal layer is deposited by chemical vapor deposition.
14. (Original) The method of claim 2 wherein the metal layer is deposited by electroplating.
15. (Original) The method of claim 1 wherein the via has an aspect ratio of about 4 to 1 and the trench has an aspect ratio of about 1 to 1.
16. (Original) The method of claim 1 wherein the second barrier layer has a thickness of from about 20 Å to about 50 Å at the bottom of the via.

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17. (Original) The method of claim 1 wherein the second barrier layer is selected from the group consisting of Ta, TaN, W, WN_x, Ti, and TiN, and the second barrier layer has a thickness of from about 20 Å to about 50 Å at the bottom of the via.
18. (Original) A method of filling one or more of a via and a trench in a patterned substrate, comprising:
- a) depositing a generally conformal first barrier layer on the patterned substrate by atomic layer deposition;
 - b) removing the first barrier layer from the horizontal surfaces of the patterned substrate;
 - c) depositing a second barrier layer by physical vapor deposition; and then
 - d) depositing one or more conductive materials.
19. (Original) The method of claim 18 wherein depositing the conductive material comprises depositing a seed layer and a metal layer in the via and/or the trench after the second barrier layer is deposited.
20. (Original) The method of claim 19 wherein the first barrier layer is selected from the group consisting of Ta, TaN, W, and WN.
21. (Original) The method of claim 20 wherein the second barrier layer is selected from the group consisting of Ta, TaN, TiSiN_x, TaSiN_x, W, and WN_x.
22. (Original) The method of claim 21 wherein the seed layer is copper.
23. (Original) The method of claim 22 wherein the metal layer is copper.
24. (Original) The method of claim 18 wherein the first barrier layer is deposited and removed from the horizontal surfaces of the patterned substrate within a single chamber of an integrated processing tool.

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25. (Original) The method of claim 24 wherein the chamber is an atomic layer deposition chamber and the first barrier layer is deposited and etched in the chamber.
26. (Original) The method of claim 19 wherein the seed layer is deposited by physical vapor deposition.
27. (Original) The method of claim 19 wherein the seed layer is deposited by chemical vapor deposition.
28. (Original) The method of claim 19 wherein the seed layer is deposited by electroless deposition.
29. (Original) The method of claim 19 wherein the metal layer is deposited by physical vapor deposition.
30. (Original) The method of claim 19 wherein the metal layer is deposited by chemical vapor deposition.
31. (Original) The method of claim 19 wherein the metal layer is deposited by electroplating.
32. (Original) The method of claim 18 wherein the via has an aspect ratio of about 4 to 1 and the trench has an aspect ratio of from about 1 to about 1.
33. (Original) The method of claim 18 wherein the second barrier layer has a thickness of from about 20 Å to about 50 Å at the bottom of the via.
34. (Original) The method of claim 18 wherein the second barrier layer is selected from the group consisting of Ta, TaN, W, WN_x, Ti, and TiN, and the second barrier layer has a thickness of from about 20 Å to about 50 Å at the bottom of the via.

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35. (Original) A method of filling one or more of a via and a trench in a patterned substrate having an etch stop at the via level, comprising:

- a) depositing a generally conformal first barrier layer on the patterned substrate by chemical vapor deposition;
- b) removing the first barrier layer from the horizontal surfaces of the patterned substrate;
- c) removing the etch stop from the bottom of the via;
- d) depositing a second barrier layer by physical vapor deposition; and then
- e) depositing one or more conductive materials.

36. (Original) The method of claim 35 wherein depositing the conductive material comprises depositing a seed layer and a metal layer in the via and/or the trench after the second barrier layer is deposited.

37. (Previously Presented) A method of filling one or more of a via and a trench in a patterned substrate having a metal layer underlying the via, comprising:

- a) depositing a generally conformal first barrier layer on the patterned substrate by chemical vapor deposition, wherein the first barrier layer is selected from the group consisting of TiSi_xN , $\text{TiN}(\text{C})$, $\text{TiNSi}(\text{C})$, Ta , TaC , $\text{TaN}(\text{C})$, $\text{TaNSi}(\text{C})$, W , WN_x , SiO_xN_y , SiC , AlN , and Al_2O_3 ;
- b) removing the first barrier layer from the horizontal surfaces of the patterned substrate;
- c) depositing by physical vapor deposition a second barrier layer sufficient to provide a barrier on the bottom of the trench without significantly impairing conduction between the conductive material deposited in the via and the metal layer; and then
- d) depositing one or more conductive materials.

38. (Original) A method of filling one or more of a via and a trench in a patterned substrate having a metal layer underlying the via, comprising:

- a) depositing a generally conformal first barrier layer on the patterned substrate by atomic layer deposition;

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- b) removing the first barrier layer from the horizontal surfaces of the patterned substrate;
- c) depositing by physical vapor deposition a second barrier layer sufficient to provide a barrier on the bottom of the trench without significantly impairing conduction between the conductive material deposited in the via and the metal layer ; and then
- d) depositing one or more conductive materials.

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REMARKS

This amendment is filed to correct the dependency of claim 5 to provide antecedent basis for the phrase "seed layer" in claim 5. Applicants believe that no new matter has been introduced in this response. Entry of the amendment is respectfully requested.

Respectfully submitted,



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DATE: March 4, 2004
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TO: Examiner: Ginette Peralta
FAX NO: 703-872-8306
COMPANY: USPTO
FROM: Keith M. Tackett
PAGE(S) with cover: 1
ORIGINAL TO FOLLOW? ☐ YES ☒ NO

RULE 312 AMENDMENT AFTER ALLOWANCE

TITLE: Reliability Barrier Integration for CU Application
U.S. SERIAL NO.: 07052,681
FILING DATE: January 17, 2002
INVENTOR: Q, et al.
EXAMINER: Ginette Peralta
GROUP ART UNIT: 814
CONFIRMATION NO.: 1083

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TITLE:	Integrating Barrier Integration for GUI Applications
U.S. SERIAL NO.:	0/052,681
FILING DATE:	January 17, 2002
INVENTOR:	Ch, et al.
EXAMINER:	Elnette Peralta
GROUP ART UNIT:	2814
CONFIRMATION NO.:	1083
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COMPANY: USPTO
FROM: Keith M. Tackett
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SUBMISSION OF REPLACEMENT DOCUMENTS

TITLE: Reliability Barrier Integration for CU Application
U.S. SERIAL NO.: 10/052,681
FILING DATE: January 17, 2002
INVENTOR: Xi, et al.
EXAMINER: Ginette Peralta
GROUP ART UNIT: 2814
CONFIRMATION NO.: 4083

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PATENT
Atty. Dkt. No. AMAT/1931.P1/CPI/COPPER/PJS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Xi, et al.

Serial No.: 10/052,681

Confirmation No.: 4083

Filed: January 17, 2002

For: Reliability Barrier Integration CU
Application

Group Art Unit: 2814

Examiner: Ginette Peralta

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Applicants note that while the issue fee for the instant application was paid on March 31, 2004, the instant application has not yet issued. The Examiner indicated in a telephone conversation on February 1, 2005 that the issue fee payment and the amendments after allowance filed on March 4, 2004 and March 26, 2004 have been received by the Patent Office, but have not been matched with the file.

Applicants are submitting a copy of the issue fee transmittal and the return receipt postcard indicating that the issue fee transmittal was received by the Patent Office on April 5, 2004. Applicants are also submitting a copy of the amendment after allowance filed March 4, 2004, with its facsimile confirmation and a copy of the amendment after allowance filed March 26, 2004, with its facsimile confirmation.

Applicants are submitting the attached copies to replace the misplaced issue fee transmittal and amendments after allowance to help expedite the issuance of the patent for the instant application.

Respectfully submitted,



Keith M. Tackett
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 Maureen Walstra (Signature)
 3/31/04 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,681	01/17/2002	Ming Xi	AMAT/1931.P1.CPI/ALUMINUM	4083

TITLE OF INVENTION: RELIABILITY BARRIER INTEGRATION FOR CU APPLICATION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
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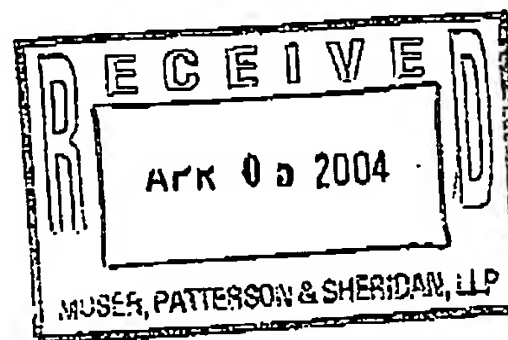
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Inventor Ming XI# et al

Serial No 10/052,681

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